METHOD FOR PREPARING INTEGRATED CIRCUIT MODULES FOR ATTACHMENT TO PRINTED CIRCUIT SUBSTRATES

Background of the Invention

I. **Field of the Invention:** This invention relates generally to methods of manufacturing electronic circuit assemblies, and more particularly to a method of semiconductor packaging of single or multiple die using tape automated bonding tape for test and elevated temperature cycling (burn-in) of such semiconductor packages.

II. **Discussion of the Prior Art:** As integrated circuit (IC) chips are made smaller and of increased complexity and as clock speeds become higher and higher, methods had to be developed to provide a suitable interconnection between the IC chips and printed circuit substrates on which such IC chips are mounted. To address the complexity and size constraints imposed, electronic packaging engineers earlier devised a process called tape automated bonding, often referred to by the acronym TAB. Tape Automated Bonding (TAB) is an inner connect technology between integrated circuits and associated substrates wherein a prefabricated carrier with copper leads adapted to the IC pads instead of individual wires. This prefabricated carrier or tape consists of a perforated polyimide film, like camera film, and of the same dimensions, which has a transport perforation and stamped openings for the IC and the connection leads. A copper foil is glued to the film and the copper is etched using photolithography. TAB is an approach to reduce the pitch and to speed up interconnection of IC chips to a lead frame, especially for high-volume production applications. There are several types of copper/polyimide composite film materials that have been found quite suitable. The polyimide sheet material is laminated with the copper foil using a thermosetting adhesive. The copper is appropriately masked and etched using well-known techniques to define inner and outer pad areas connected by fine, closely spaced conductive traces. Vias through the thickness dimension of the tape are formed and the vias are appropriately metallized, such as by electroless copper plating or by a direct metallization process (DMP) which are the thru-hole copper plating processes that involve conductive thin film deposition on the organic polymer

surface of the thru-hole wall and copper electroplating on it. The conductive traces on an undersurface of the TAB tape individually lead to a plurality of solder ball mounting pads commonly referred to as a ball grid array (BGA) that facilitate attachment of integrated circuit chips mounted on the TAB tape to a printed circuit substrate.

In accordance with the prior art and as reflected by the flow chart of Figure 1, wire bonding techniques are used to connect a fine wire between an on-chip I/O pad and a pad on the TAB tape. Once all of the wire bonds are established, the semiconductor die or dies are overmolded with a plastic encapsulant, after which solder balls are attached to the pads in the BGA located on the undersurface of the TAB tape beneath the die.

Following the teachings of the prior art, the TAB tape is then severed about the perimeter of the integrated circuit to yield discrete chips. The discrete chips are then placed in a custom made ball grid socket so that testing and burn-in can be performed on the chip before it is mounted in the end device using a reflow solder technique to join the solder balls of the BGA to the printed circuit board of the end device.

BGA sockets used for test and burn-in are dependent on ball pitch, ball size and the package outline. Any variation from the standard results in an expensive, custom test socket. Burn-in of BGAs often results in deformation of the solder balls. In that BGA test sockets require a specific ball size, any change in ball size results in the need for retooling of the BGA sockets. This necessarily increases the manufacturing cost of an integrated circuit assembly.

In accordance with the present invention semiconductor I/O are routed on TAB tape first to BGA pads internal to the die outline and secondly to test pads located external to the semiconductor package outline. In this fashion, the test pads can be used during test and burn-in, making it unnecessary to have expensive BGA sockets in order to do the test and burn-in. The method of the present invention also eliminates the need to contact the solder balls on the BGA during testing and burn-in so that they remain properly spaced and shaped for later reflow solder attachment to mating pads on a printed circuit assembly.

SUMMARY OF THE INVENTION

The present invention comprises a method of preparing an integrated circuit module for attachment to a printed circuit substrate and involves the steps of providing a TAB tape frame having a predetermined conductive test pad footprint formed about a perimeter of the TAB tape frame and a bond pad footprint generally centrally disposed relative to the test pad footprint and that has conductive leads connecting the bond pads individually to the test pads as well as to BGA pads that are centrally disposed relative to the bond pad footprint. One or more semiconductor dies comprising integrated circuits are affixed to the TAB tape frame. Input/output points of the integrated circuits are wire-bonded to the selected ones of the bond pads in the bond pad footprint. Following that, the semiconductor die or dies and the bond pad footprint are overmolded with plastic to form the encapsulated integrated circuit module. Before cutting the integrated circuit module free of the TAB tape, testing and burn-in are performed on the integrated circuit by connecting test probes of an automated circuit tester to the conductive test pads in the test pad footprint.

As a further step in the method, solder balls may be applied to the ball grid array pads prior to the testing and burn-in step. Only after such test and burn-in operations are completed is the tab tape severed about the over-molded semiconductor die to extract the circuit module which then may be affixed to a printed circuit substrate by reflow soldering the solder balls on the ball grid array to conductive pads on the printed circuit board.

DESCRIPTION OF THE DRAWINGS

The foregoing features, objects and advantages of the present invention will become apparent to those skilled in the art from the following detailed description of a preferred embodiment, especially when considered in conjunction with the accompanying drawings in which:

Figure 1 is a process flow chart illustrating the prior art processing method for preparing an integrated circuit module for attachment to a printed circuit substrate;

Figure 2 is a process flow chart of the improved method in accordance with the present invention;

Figure 3A shows an uncased semiconductor die bonded to a TAB tape with wire bonds connecting input/output points on the die with selected ones of the bond pads;

Figure 3B shows the device of Figure 3A following the overmolding of the die and bond pads with plastic;

Figure 3C is a view of the underside of the assembly of Figure 3B showing solder balls attached to the BGA;

Figure 3D illustrates the IC, still mounted on the TAB tape at the time of test and burn-in;

Figure 3E shows the finished integrated circuit package after it has been stamped out from the TAB tape frame; and

Figure 3F shows the device of Figure 3E mounted on a printed circuit board by reflow soldering of the solder balls.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to Figure 2, the method of the present invention is expressed in the flow chart presented there. The first step in the process is to fabricate or procure from a vendor TAB tape, one frame of which is shown in the view of Figure 3A. As explained earlier, it comprises a flexible polyimide substrate 10 having conductive traces 12 leading from a plurality of discrete test pads arranged in a pattern 14 in accordance with the standard EIAJ ED-7134A entitled "General Rules for the Preparation of Outline Drawings of Integrated Circuit Quad Tape Carrier Packages" proximate the perimeter of the frame to a plurality of bond pads as at 16 that also lie in a generally rectangular footprint that is centrally disposed relative to the test pad footprint 14.

Referring momentarily to Figure 3C, which shows the obverse side of the TAB tape frame, the conductive lines 12 not only connect the bond pads 16 individually to the test pads in footprint 14, but they also connect to ball grid array pads 18 that are generally centrally disposed relative to the bond pad footprint.

Referring again to Figure 3A, and to the flow chart of Figure 2, the next step in the process is to place a semiconductor die 20 on the tab tape within the confines of

the bond pad footprint and to affix it in place with a suitable bonding agent such as epoxy. While the view of Figure 3A shows an arrangement where two semiconductor dies are stacked to form a multi-chip module (MCM), those skilled in the art will appreciate that only a single die can be used in practicing the method of the present invention.

Once the semiconductor dies are placed and attached and the epoxy is allowed to cure, the next step in the process is to wire bond tie points on the semiconductor die(s) to ones of the inner bond pads 16. Here, fine gold or aluminum wires are temperature and compression bonded to tie points on the semiconductor die(s) and to bond pads on the TAB tape substrate using well-known techniques.

Once the wire bonding step has been completed, the bare semiconductor die(s) is/are overmolded with a suitable plastic, such as an epoxy, where the overmolding not only encapsulates the semiconductor die(s), but also the wire bond footprint. An approach commonly used to effect encapsulation is to first create a dam around the semiconductor die to define an area. The encapsulant as well as the substrate may be preheated to desired temperatures and a quantity of the encapsulant is dispensed around the bonding areas. Subsequently, the encapsulant is applied to fill in the complete area. In a dam & fill encapsulation process, the substrate is preheated to a temperature of about 100° C and a high viscosity encapsulant is dispensed to form a high dam around the chip to define the area to be covered. Next, a low viscosity encapsulant is dispensed into the dammed area such that a very flat encapsulation profile is achieved. However, because the dam and fill technique, at times, does not create a well-defined edge along which a cut can be made, I prefer to use a conventional injection overmolding technique to achieve encapsulation. The overmolded die and bonding pads are shown in the view of Figure 3B.

As is reflected in the flowchart of Figure 2, the next step in the process is to attach solder balls to the BGA. As has already been explained, traces from the bond pads connect to thru-hole vias that extend to the bottom of the substrate and conductively join to circular solder pads on the bottom surface. As shown in Figure 3C, the bottom side solder pads are laid out in a square or rectangular grid format with

a predetermined pitch. Solder balls of a predetermined size are then reflow soldered to the BGA pads. The view of Figure 3C shows the solder balls already attached to underlying BGA pads printed on the undersurface of the TAB substrate.

At this point, rather than severing the die from the TAB tape, the assembly of Figure 3C is subjected to test & burn-in procedures where the assembly is raised to a somewhat elevated temperature and the test pads 14 are probed with a "bed-of-nails"-type tester whereby signals and operating potentials are applied to the encased chip by way of the conductive traces 12 and the wire bond connections and, likewise, output signals are picked up by the test probes from the test pads 14. By utilizing the test pads 14 rather than a custom BGA socket to establish contact between the encased semiconductor die and the external test equipment, there is no risk of deformation of the solder balls even when high temperatures are applied during the burn-in process. This better ensures that the solder balls will not be distorted, permitting a more precise match when the integrated circuit chip is to be reflow soldered to a printed circuit board.

Following the test and burn-in procedure, the encapsulated integrated circuit chip is singulated, i.e., cut free of the TAB frame. A stamping technique is preferably used to achieve singulation. The finished MCM is shown in Figure 3E.

Figure 3F shows the chip of Figure 3E mounted on a printed circuit board where the solder balls are reflow soldered so as to attach to printed circuit terminals on the substrate 22.

Whereas in the prior art method burn-in and test of BGAs involves contact the solder balls with a test socket that often causes the balls to deform during high temperature, the practice of the method of the present invention avoids changes in ball size and spacing, making it unnecessary to retool BGA sockets, as is often the case when the prior art method is utilized. Because the test probes are only made to engage the test pads of test pad footprint 14, a custom socket for mating with the BGA is unnecessary. Furthermore, the present invention allows for shaped packages that conform to odd assembly shapes in that ball location does not need to be on a standard grid nor is it necessary that the solder ball size be uniform as is the case when a BGA

socket is used to interface the circuit tester with the IC.

This invention has been described herein in considerable detail in order to comply with the patent statutes and to provide those skilled in the art with the information needed to apply the novel principles and to construct and use such specialized components as are required. However, it is to be understood that the invention can be carried out by specifically different equipment and devices, and that various modifications, both as to the equipment and operating procedures, can be accomplished without departing from the scope of the invention itself.

What is claimed is: